

The diagram illustrates a multiprocessor system architecture. On the left, four identical processor units are stacked vertically. Each unit contains a 'PROCESSOR' block with a 'CACHE' and an 'OS' (Operating System) component, specifically labeled 'DOS'. These processors are connected to a central 'MP/MDD SYSTEM' bus. To the right of the bus, there is a vertical stack of control and mapping components: 'BINDING', 'BINDING MAPPER', and 'ADDRESS MAPPER' (which contains an 'ADDRESS MAP'). These are connected to the bus and to each other via bidirectional arrows. Below the bus, four 'ADAPTER' blocks are connected to the processors. An 'INTER-PROCESSOR BUS' is shown connecting the adapters. To the right of the adapters, there are four 'AP' (Application Processor) blocks, each connected to an adapter. These AP blocks are connected to a 'SWITCH' block, which in turn connects to four 'DP' (Data Processor) blocks. Each DP block is connected to a 'DISK DRIVE'. At the top right, a block labeled 'A/DDC PROGRAMS' is connected to the 'SWITCH' and the 'ADDRESS MAPPER' via bidirectional arrows.

FIG. 1
PRIOR ART

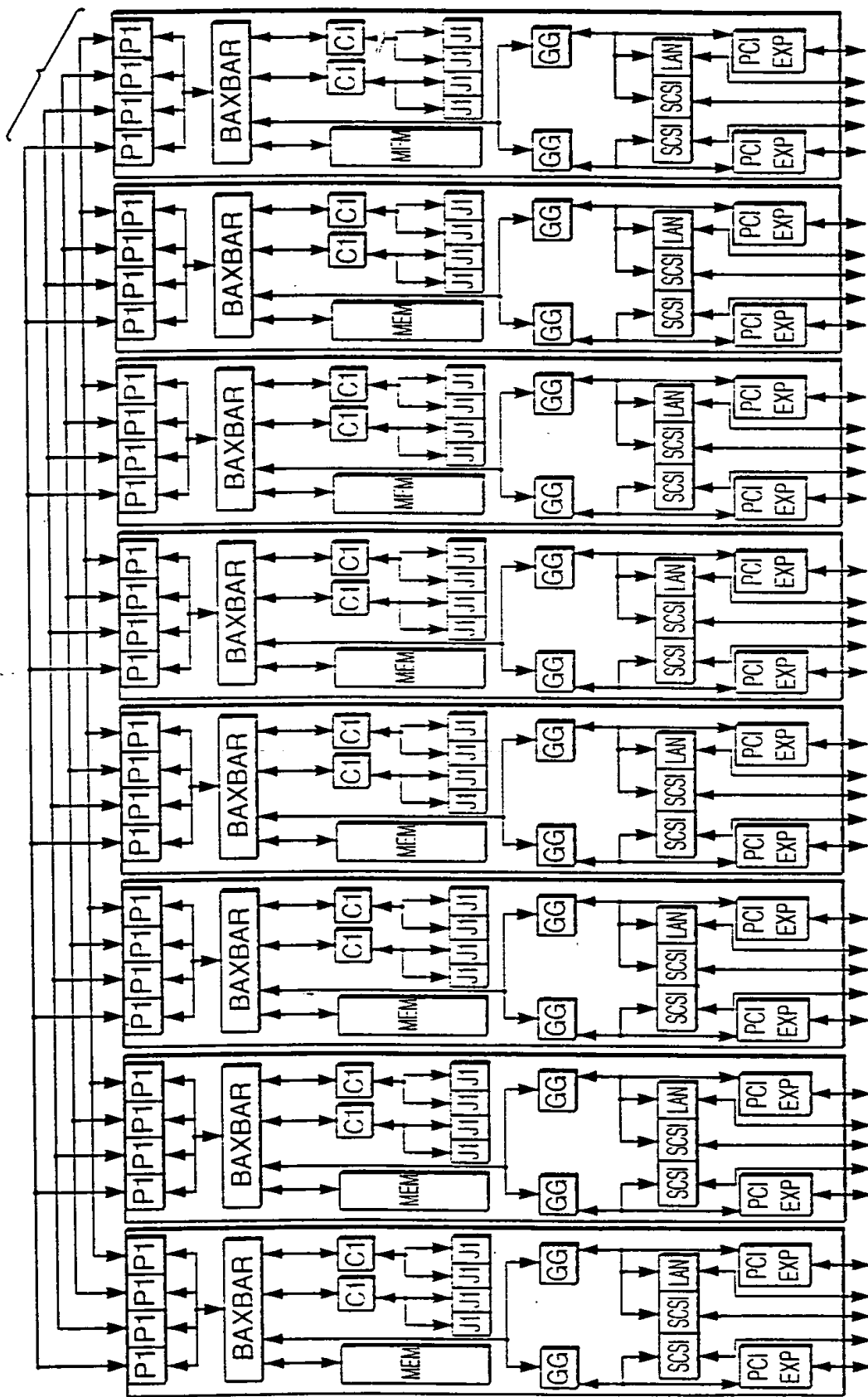


FIG. 2
PRIOR ART

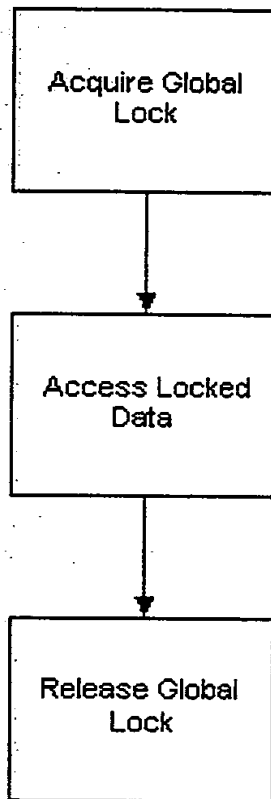


FIG. 3
PRIOR ART

006260" 96E5/960

00675396-092900

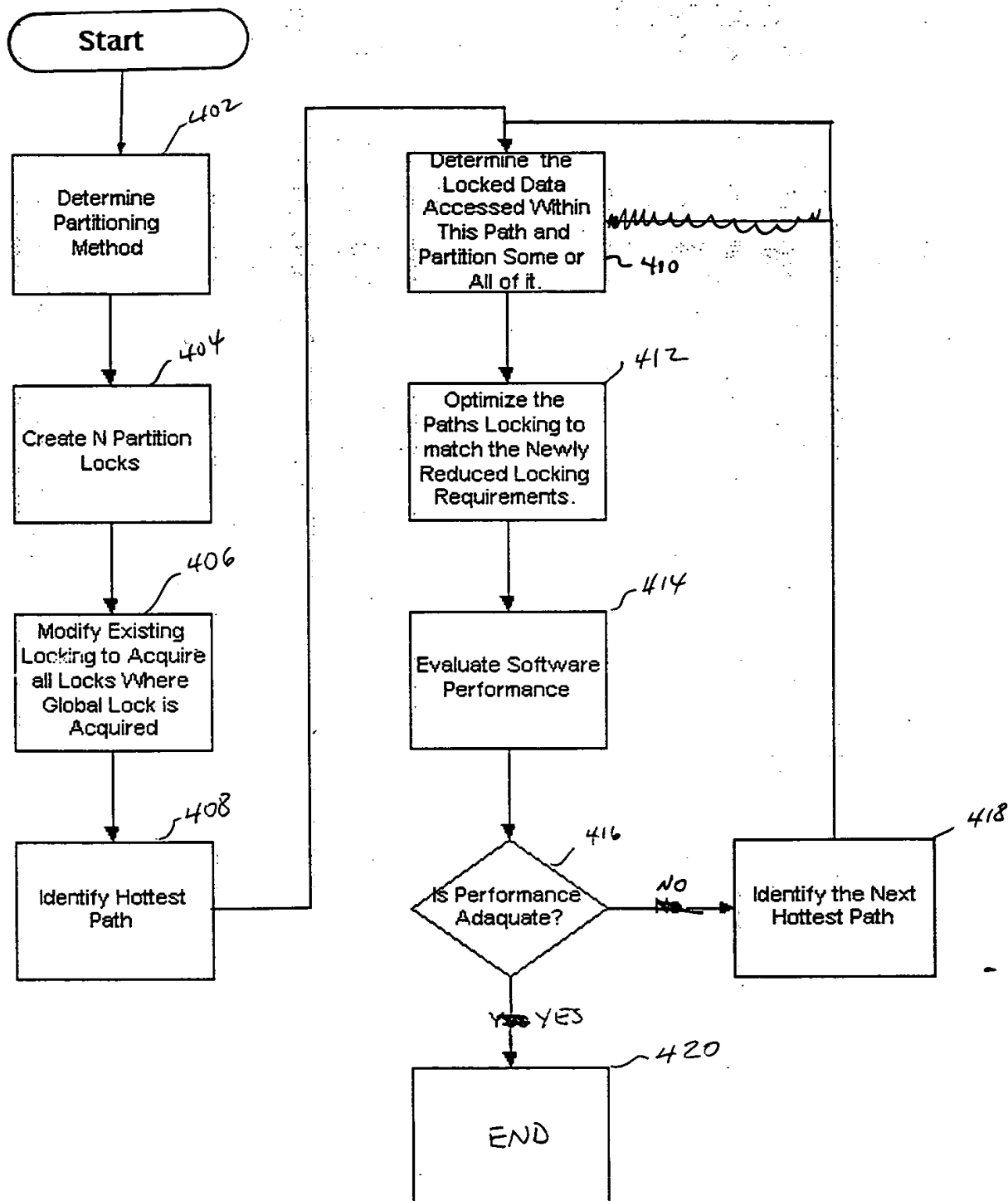


FIG. 4

Fig 5A

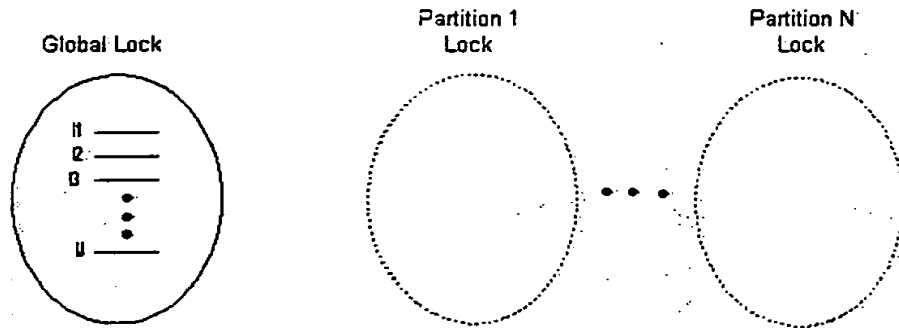


Fig 5B

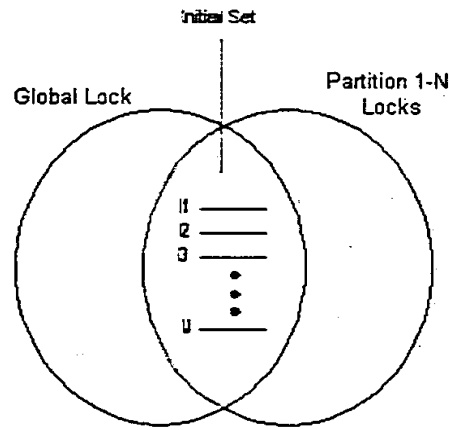
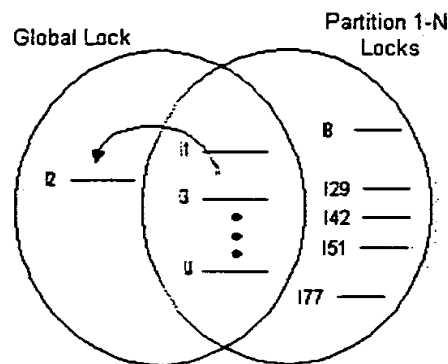


Fig 5C



006260" 96E52950

Acquire Partition
Locks 1-N

502

Acquire Global
Lock

504

Access Locked
Data

506

Release Partition
Locks 1-N

508

Release Global
Lock

510

FIG. 6

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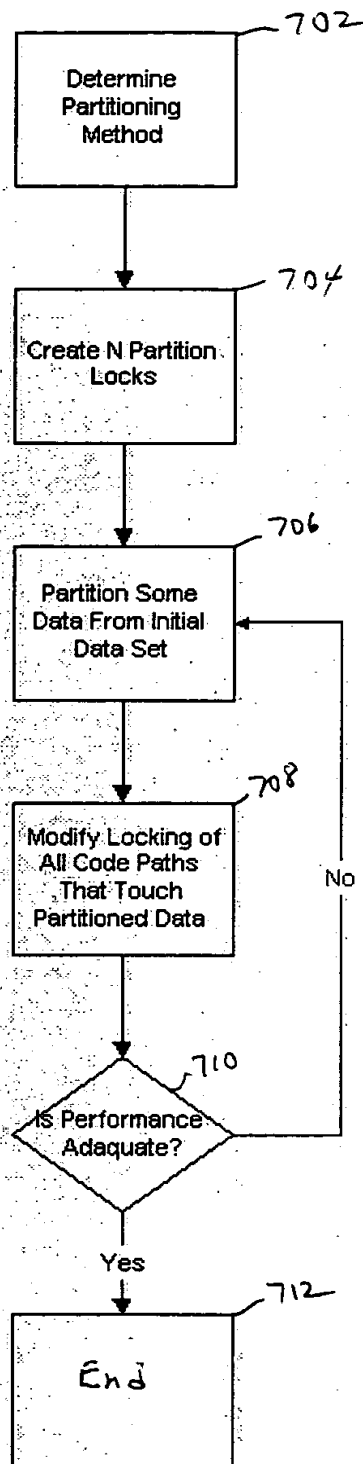


Fig 7